**Shannon Systems Nor-Flash Control Spec**

**(Flash\_spi\_g5)**

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**Shannon Systems.**

**Checked by:**

**Approved by:**

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General Description

Flash\_spi\_g5 module mainly realizes the function of controlling Nor Flash, such as read, write and erase. It is connected to upper level by HOSTBUS, and communicating with Nor Flash device by SPI wires. Its core task is to translate HOSTBUS orders into SPI order sequences for Nor Flash.

Feature List

* After input reset\_ down, the module will wait for Nor\_Flash initial, then send back initial\_done high to upper level.
* The module uses rd\_ram and wr\_ram as buffer to read from and write to Nor Flash device. Write operation unit is one page, and read operation unit is one sector (1024 DWORD).
* Host\_address range should be 16’h1000 to 16’h1400 to conduct a NorFlash read / write operation.
* Host\_address[5:0] is order and state indicator.
* When host\_be and host\_req are high, and host[5:0] is 1D, host\_datain[31], [30], [29] are used as erase, program and erase flag individually.
* Typically, spi\_sck is 250MHz/8=31.25MHz, and can also be configured.

Pin List and Assignment

Interface Diagram

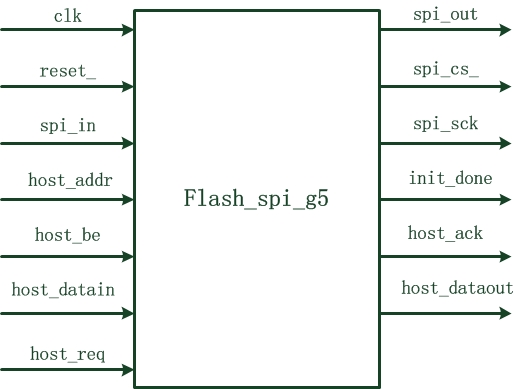


Figure 1 Flash\_spi\_g5 Pin Assignment Diagram

Pin List Table

|  |  |  |
| --- | --- | --- |
| Name | IO | Description |
| **Input** | | |
| clk | I | Sytem clock(core clock domain) |
| reset\_ | I | Module reset |
| spi\_in | I | Spi data input |
| host\_addr[15:0] | I | Address signals of host bus |
| host\_be[3:0] | I | Write enable signals of host bus |
| host\_datain[31:0] | I | Host data in |
| host\_req | I | Host request |
| **Output** | | |
| spi\_out | O | Spi data output |
| spi\_cs\_ | O | Nor Flash chip select signal |
| spi\_sck | O | Spi serial clock to Nor Flash |
| init\_done | O | Nor Flash initial done indicator signal |
| host\_ack | O | Host acknowledge |
| host\_dataout[31:0] | O | Host data out |

# Block Diagram

Block Diagram

The block diagram is displayed as Figure 2.

## Block Description

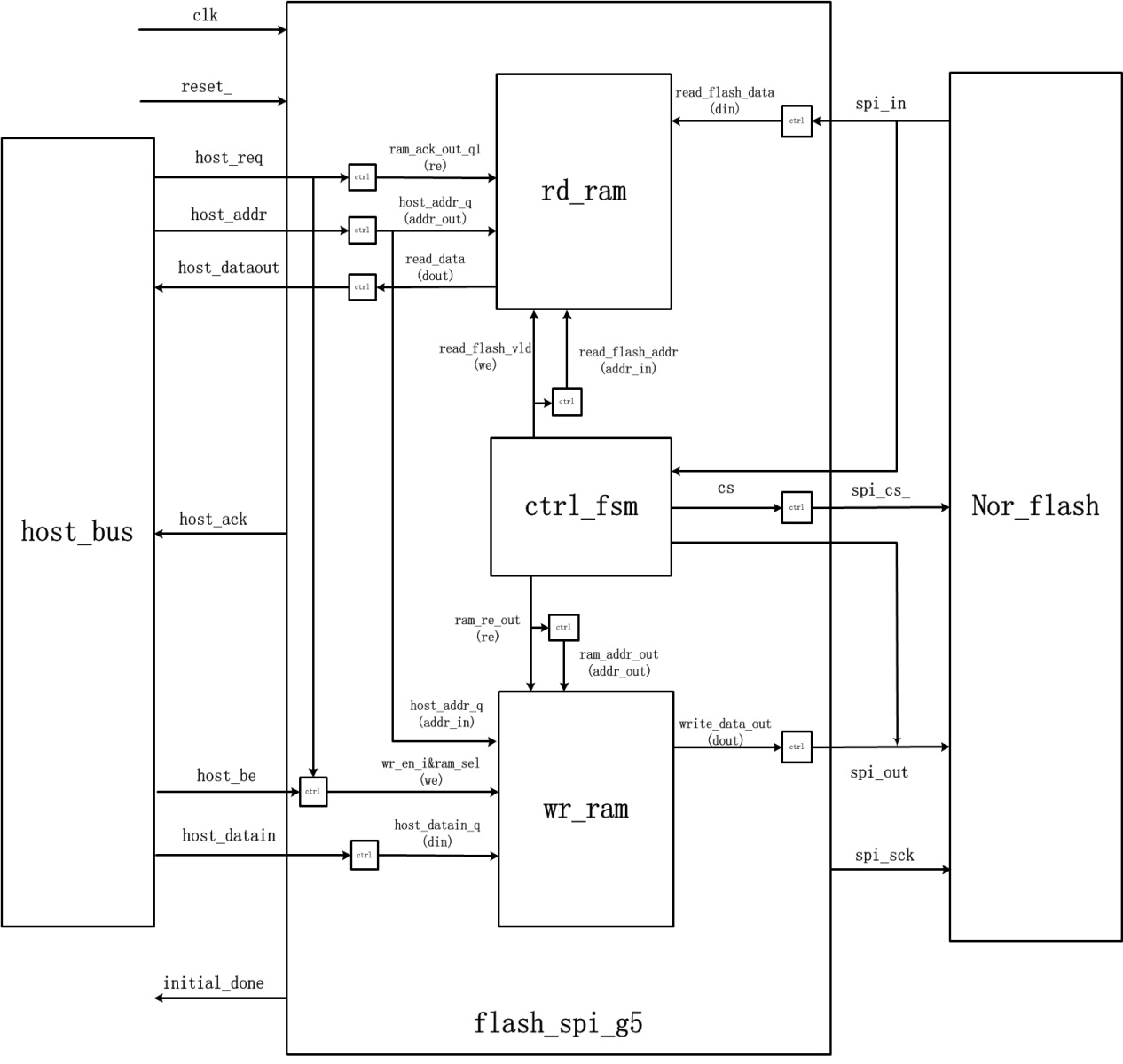
rd\_ram

Rd\_ram worked as a buffer to read from Nor Flash. Its data-in get read data from spi\_in wire, and the data is read to host\_dataout.

Wr\_ram

Wr\_ram worked as a buffer to write to Nor Flash. Its din get data from host\_datain, and the data is read to write\_data\_out. Write\_data \_out is finaly output by spi\_out.

Both rams are controlled by input hostbus signals and the main FSM together.

**Figure 2 Flash\_spi\_g5 Diagram**

Main FSM Flow

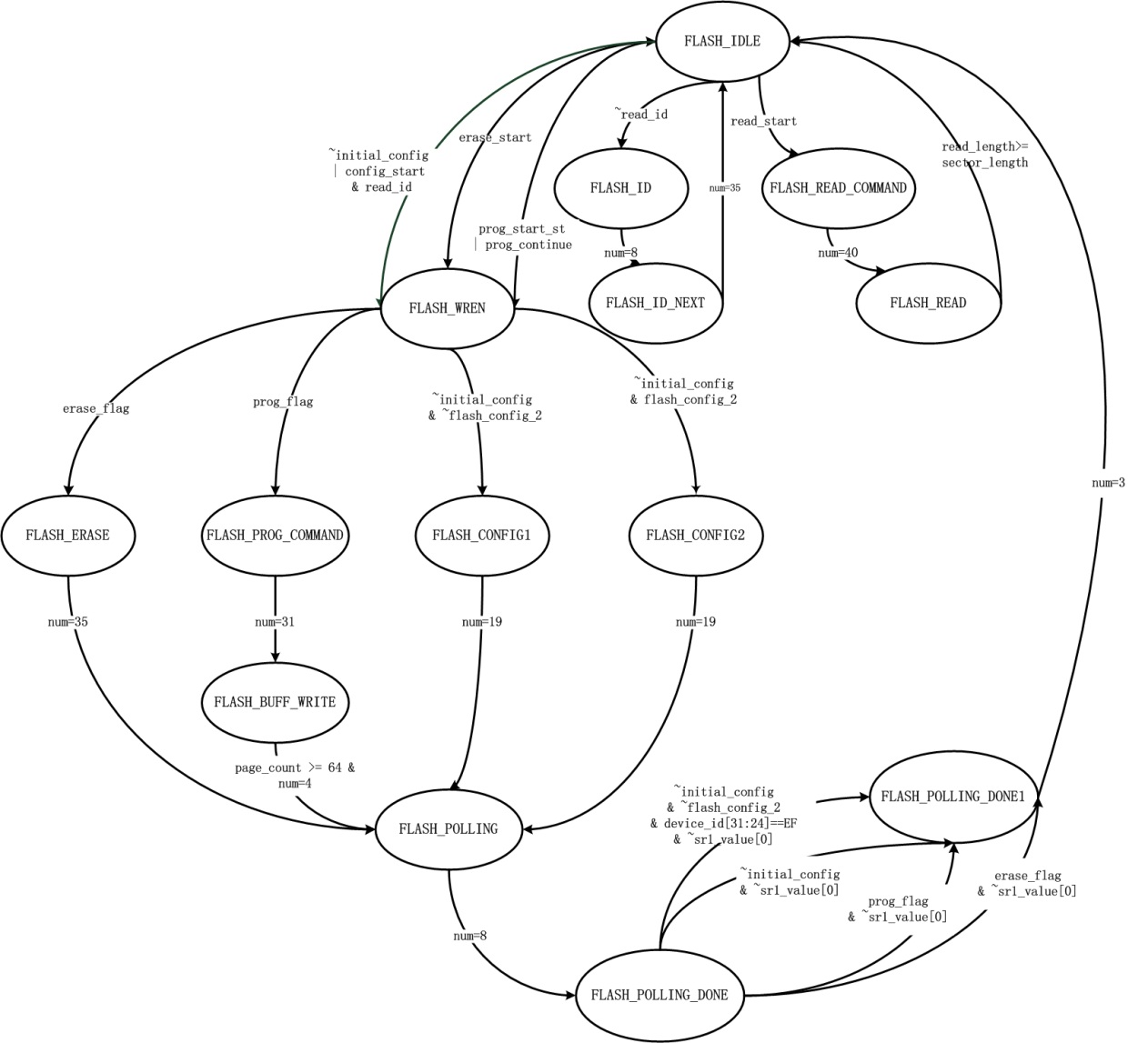


Figure 3 Nor\_control\_fsm

# Reference flow

## Default Values of Nor Flash Control Registers

The address for data buffer is from 16r1000 to 16r1400. Top level reads and writes registers from 16r1C to 16r1F to control Nor Flash. And default values of control registers are displayed in Table 1.

|  |  |  |
| --- | --- | --- |
| Address | Default(16r) | Description |
| 1C | Read only | Reflect G5 Nor Flash ID |
| 1D | 00000000 | No operation of program/  read/ erase |
| 1E | 00000001 | Engine state is done |
| 1F | 00000003 | Default sck frequency is  (System Clock) / 8 |

**Table 1 Default Values for Nor Flash Control Registers**

## Program operation

Before program operation, the program data should be written in address from 16r1000 to 16r1400 by lbi\_write. Then write DWORD 1D to start a program operation. DWORD 1D [30] is the program start flag, and DWORD 1D [15:0] is address.

**Reference operation:**

dut lbiWrite: 16r40001100 to: 16r1D.

It indicates that 4K bytes data from address 16r1100 will be written to Nor Flash.

## Read Operation

Reading operation is very similar with a program operation. The difference is that DWORD 1D[29] is the read start flag.

**Reference Operation:**

dut lbiWrite: 16r20001100 to: 16r1D.

It indicates that 4K bytes data from Nor Flash will be read to address 16r1100.

## Erase Oration

**Reference Operation:**

dut lbiWrite: 16r80000100 to: 16r1D.

It indicates that 4K bytes data of Nor Flash from address 100 will be erased.

## Get Nor Flash ID

**Reference Operation:**

dut lbiRead: 16r1C.

Nor Flash ID will be returned.

## Check Nor Flash Controller Working State

**Reference Opreation:**

dut lbiRead: 16r1E.

The return value of 1 indicates it’s busy, while 0 indicates it’s idle. Notice that no operation of read /write /erase can be conducted synchronously, which means that DWORD 1D [31], [30],[29] can’t be set 1 at the same time.

## Configure Frequency of SCK

**Reference Operation**:

dut lbiWrite: 16r2 to: 16r1F.

The frequency of SCK will be changed to (System Clock) / 6.